a first transistor having a current path coupled between the first terminal and the third terminal and having a control terminal coupled to the second terminal; and

a second transistor having a current path coupled between the second terminal and the third terminal and having a control terminal coupled to the first terminal.

22. (New) A circuit as in claim 21, wherein the device and the first and second transistors are formed at a face of a first semiconductor region having a first conductivity type.

23. (New) A circuit as in claim 22, wherein the first semiconductor region is surrounded on all sides by a second semiconductor region having a second conductivity type.

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24. (New) A circuit as in claim 22, wherein the first semiconductor region is enclosed on all sides and below by a second semiconductor region having a second conductivity type, and wherein the second semiconductor region is formed in a third region isolated from the first region.

25. (New) A circuit as in claim 21, wherein the device is an MOS transistor.

26. (New) A circuit as in claim 25, wherein the MOS transistor comprises a control terminal coupled to the third terminal.

27. (New) A circuit as in claim 25, wherein the current path of the first transistor is coupled between the first and third terminals by a first resistor and the current path of the second transistor is coupled between the second and third terminals by a second resistor.

28. (New) A circuit as in claim 25, wherein each of the MOS transistor, the first transistor, and the second transistor comprises a bulk terminal coupled to the third terminal.

29. (New) A circuit as in claim 21, wherein the device is a bipolar transistor.

30. (New) A circuit as in claim 29, wherein the bipolar transistor comprises a control terminal coupled to the third terminal.

31. (New) A circuit as in claim 30, wherein each of the first and second transistors comprises a bulk terminal coupled to the third terminal.

32. (New) A circuit as in claim 29, wherein the current path of the first transistor is coupled between the first and third terminals by a first resistor and the current path of the second transistor is coupled between the second and third terminals by a second resistor.

33. (New) A circuit as in claim 21, wherein the device comprises a plurality of parallel elongate semiconductor regions having a first conductivity type, and wherein the current path of the device comprises a plurality of semiconductor regions having a second conductivity type formed between respective said semiconductor regions having the first conductivity type.

34. (New) A circuit, comprising:

a first terminal;

a second terminal;

a third terminal;

a first device having a current path coupled between the first and second terminals;

a second device having a current path coupled between the first terminal and the third terminal, the second device current path not conducting in response to a positive voltage at the first terminal with respect to the second terminal and conducting in response to the positive voltage at the second terminal with respect to the first terminal; and

a third device having a current path coupled between the second terminal and the third terminal, the third device current path conducting in response to the positive voltage at the first terminal with respect to the second terminal and not conducting in response to the positive voltage at the second terminal with respect to the first terminal.

35. (New) A circuit as in claim 34, wherein the first, second, and third devices are formed at a face of a first semiconductor region having a first conductivity type.

36. (New) A circuit as in claim 35, wherein the first semiconductor region is surrounded on all sides by a second semiconductor region having a second conductivity type.

37. (New) A circuit as in claim 35, wherein the first semiconductor region is enclosed on all sides and below by a second semiconductor region having a second conductivity type, and wherein the second semiconductor region is formed in a third region isolated from the first region.

A1 38. (New) A circuit as in claim 34, wherein the first device is an MOS transistor.

39. (New) A circuit as in claim 38, wherein the MOS transistor comprises a control terminal coupled to the third terminal.

40. (New) A circuit as in claim 34, wherein the current path of the second device is coupled between the first and third terminals by a first resistor and the current path of the third device is coupled between the second and third terminals by a second resistor.

41. (New) A circuit as in claim 34, wherein each of the first, second, and third devices comprises a bulk terminal coupled to the third terminal.

42. (New) A circuit as in claim 34, wherein the first device is a bipolar transistor.

43. (New) A circuit as in claim 42, wherein the bipolar transistor comprises a control terminal coupled to the third terminal.

44. (New) A circuit as in claim 43, wherein the current path of the second device is coupled between the first and third terminals by a first resistor and the current path of the third device is coupled between the second and third terminals by a second resistor.

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45. (New) A circuit as in claim 34, wherein the first device comprises a plurality of parallel elongate semiconductor regions having a first conductivity type, and wherein the current path of the first device comprises a plurality of semiconductor regions having a second conductivity type formed between respective said semiconductor regions having the first conductivity type.